Specification Amendments

Please replace paragraph 002 with the following rewritten paragraph:

002 As devices become smaller and integration density increases, reactive ion etching (RIE) has become a key process in anisotropic etching of semiconductor features. RIE or ion-enhanced etching works by a combination of physical and chemical mechanisms for achieving selectivity and anisotropicity during the etching process. Generally, plasma assisted etching operates in the milliTorr range and above. Generally, three processes compete with each other during plasma etching; physical bombardment by ions, chemical etching by radicals and ions, and surface passivation by the deposition of passivating films. In some applications, for example, high density plasmas (HDP) having a higher density of ions and operating at lower pressures ~~has~~ have been increasingly used in etching processes. Please replace paragraph 007 with the following rewritten paragraph:

Please replace paragraph 005 with the following rewritten paragraph:

005 Another problem with prior art processes, is that the use of fluorine containing plasmas in photoresist removal processes tends to preferentially etch through the oxide layer which is formed over the source and drain regions to moderate the ion implantation energies and protect the underlying silicon. As a result, plasma etching damage to the underlying silicon frequently results including etch away a portion of the silicon.

Please replace paragraph 0015 with the following rewritten paragraph:

0015 Still referring to Figure 1A, following the well region formation process, the wafer is cleaned by conventional processes to expose the silicon surface ~~by conventional processes~~ and a gate dielectric layer 16 is formed. The gate dielectric is typically formed of thermally grown SiO_2, but may also be formed of high-K dielectric materials formed over a thermally grown SiO_2 layer, for example by atomic layer CVD.

Please replace paragraph 0016 with the following rewritten paragraph:

0016 Still referring to Figure 1A, a polysilicon layer is

then deposited over the gate dielectric layer 16 to a thickness of about 1500 Angstroms to about 3000 Angstroms. The polysilicon layer is then photolithographically patterned and plasma etched according to a reactive ion etch (RIE) process to form polysilicon gate electrodes e.g., NMOS polysilicon gate electrode 18A and PMOS polysilicon gate electrode 18B. Following formation of the polysilicon gate electrodes source drain extension (SDE) regions e.g., 20A and 20B are formed adjacent the polysilicon electrodes to a shallow depth of about 30 to about 100 nm beneath the silicon surface adjacent the polysilicon electrode[[s]] sidewalls according to a low energy ion implantation or plasma immersion doping process. Conventional masking processes are used to deposit photoresist masks for respective ion implantation or plasma immersion doping of the NMOS and PMOS devices to form the SDE regions and conventional plasma ashing processes are used to remove the photoresist.

Please replace paragraph 0018 with the following rewritten paragraph:

0018 Following sidewall spacer formation, a photoresist mask 25B is deposited to cover an area including one of the NMOS or PMOS device ~~areas~~ gate areas leaving the other device, e.g. the

NMOS device 10A gate area uncovered for carrying out a high dose ion implantation (HDT) to form the high density implant source and drain regions in the silicon substrate adjacent the sidewall spacers e.g., 2622A. For example dopant atoms are implanted to a dose of about 1 to 5 x 10^{15} dopant atoms/cm^2 and at energies up to about 2 MeV to form a doped region e.g., 26A of deeper depth compared to the SDE regions e.g., 20A. The polysilicon electrodes 18A and 18B may optionally be doped at the same time the HDT is carried out to form the source and drain regions to lower a sheet resistance of the polysilicon.

Please replace paragraph 0020 with the following rewritten paragraph:

0020 Referring to Figures 1C and 1D, following the HDI implantation process of one of the CMOS devices it is necessary to remove the photoresist mask e.g., 25B prior to forming photoresist mask 25A as shown in Figure 1C and repeating the HDI process to form high density implant source and drain regions e.g., 26B in the PMOS device 10B. During the HDI processes, the high energy of the implantation ions induces cross-linking reactions to form a hardened (cross-linked) shell in the upper portion of the photoresist layer, requiring the use of fluorine

and oxygen containing plasmas to effectively etch and remove the photoresist mask e.g., 25B following a first HDI process in addition to removing photoresist mask ~~26~~25A as shown in Figure 1D, following a second HDI process to form doped source and drain regions e.g., 26[[B]]A.

Please replace paragraph 0026 with the following rewritten paragraph:

0026 Following the photoresist etching process one or more activation annealing steps or one or more high temperature annealing processes, for example at temperatures from about 600 °C to about 850 °C are carried out to activate the source and drain regions by fully or partially recrystallizing the amorphous silicon portions prior to formation of a salicide over the respective source and drain regions. Preferably the entire silicon substrate is recrystallized, for example following the salicide formation process whereby the impurity atoms are activated by being incorporated into lattice sites. After removal of any remaining silicon oxide over the source and drain regions, salicides are then formed, for example cobalt salicide, over the source and drain regions and optionally including an upper portion of the polysilicon gate electrode.